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APPLICATION BULLETIN
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TOUCH SCREEN CONTROLLER TIPS

By Skip Osgood, CK Ong, and Rick Downs

Burr-Brown makes a number of specialized analog-to-digital converters for touch screen applications. The ADS7843, ADS7845, and the new ADS7846 converters all are designed for specific touch screen applications. Applications using these devices can benefit greatly from the tips presented in this application bulletin. Most of the examples discuss the ADS7843, but the techniques shown are applicable to all of the devices.

We begin by looking at the theory of operation of a resistive touch screen, and using these specialized A/D converters with such a screen. Techniques are presented for improving accuracy and minimizing errors; the operation of the pen interrupt line (PENIRQ) is explored, ESD protection methods for the converters, and issues surrounding interfacing these converters to popular microprocessors are discussed.

RESISTIVE TOUCH SCREENS

A resistive touch screen works by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where a screen is touched by an input stylus, pen, or finger. The change in the resistance ratio marks the location on the touch screen.

The two most popular resistive architectures use 4-wire or 5-wire configurations (as shown in Figure 1). The circuits determine location in two coordinate pair dimensions, although a third dimension can be added for measuring pressure in 4-wire configurations.

THE 4-WIRE TOUCH SCREEN COORDINATE PAIR MEASUREMENT

A 4-wire touch screen is constructed as shown in Figure 2. It consists of two transparent resistive layers.

The 4-wire touch screen panel works by applying a voltage across the vertical or horizontal resistive network. The A/D converts the voltage measured at the point the panel is touched. A measurement of the Y position of the pointing device is made by connecting the X+ input to a data converter chip, turning on the Y+ and Y– drivers, and digitizing the voltage seen at the X+ input. The voltage

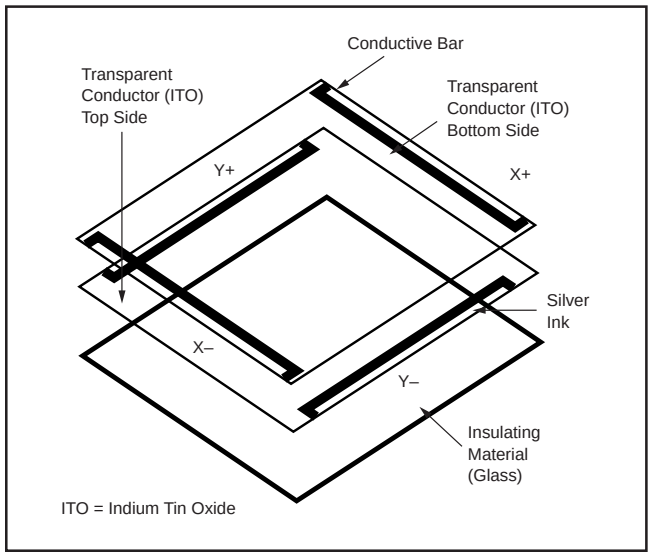

FIGURE 2. 4-Wire Touch Screen Construction.

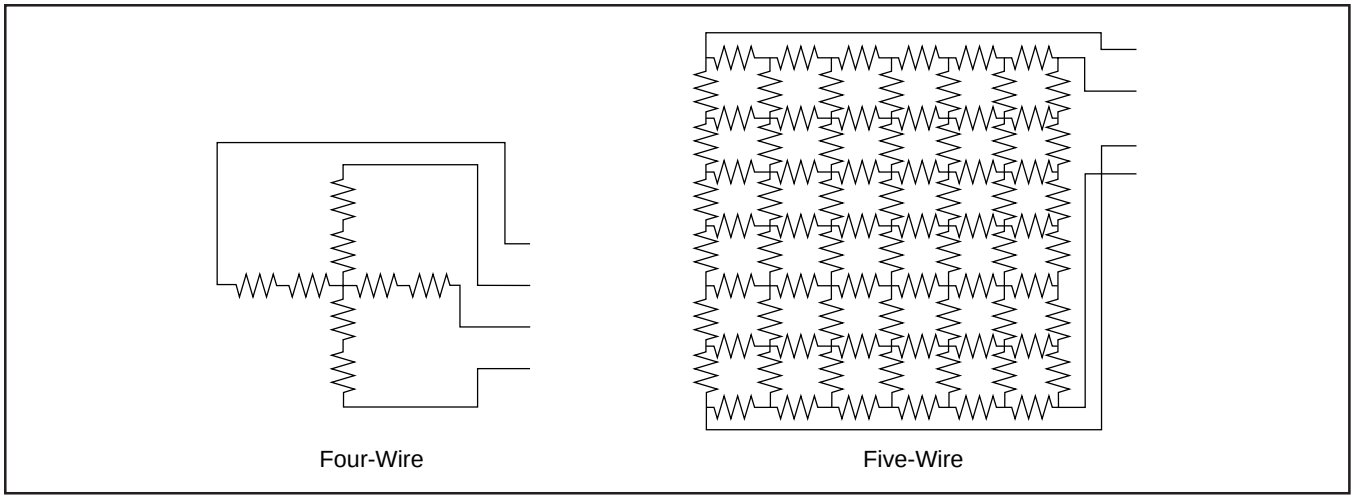

FIGURE 1. 4-Wire and 5-Wire Touch Screen Circuits.

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measured is determined by the voltage divider developed at the point of touch. For this measurement, the horizontal panel resistance in the X+ lead doesn't affect the conversion due to the high input impedance of the A/D converter.

Voltage is then applied to the other axis, and the A/D converts the voltage representing the X position on the screen through the Y+ input. This provides the X and Y coordinates to the associated processor.

THE 5-WIRE TOUCH SCREEN COORDINATE PAIR MEASUREMENT

A 5-wire touch screen is constructed as shown in Figure 3. The resistive panel consists of one transparent resistive layer and a top metal contact area separated by insulating spacers.

The 5-wire touch screen panel works by applying a voltage at the corners of the bottom resistive layer and measuring the vertical or horizontal resistive network with the wiper, or 5th wire. The A/D converts the voltage measured at the wiper point the panel is touched. A measurement of the Y position of the pointing device is made by connecting the upper left and upper right corners of the resistive layer to V+ and the lower left and lower right corners to ground. This biases the panel for a vertical deflection input to the data converter chip, and is measured by the A/D converter through the wiper touch point to the panel. The voltage measured is determined by the voltage divider developed at the point of touch. For the horizontal measurement, the upper left corner and lower left corner are connected to ground and the upper right and lower right corners are connected to V+ through the drivers and the wiper input is converted representing the horizontal deflection of the panel.

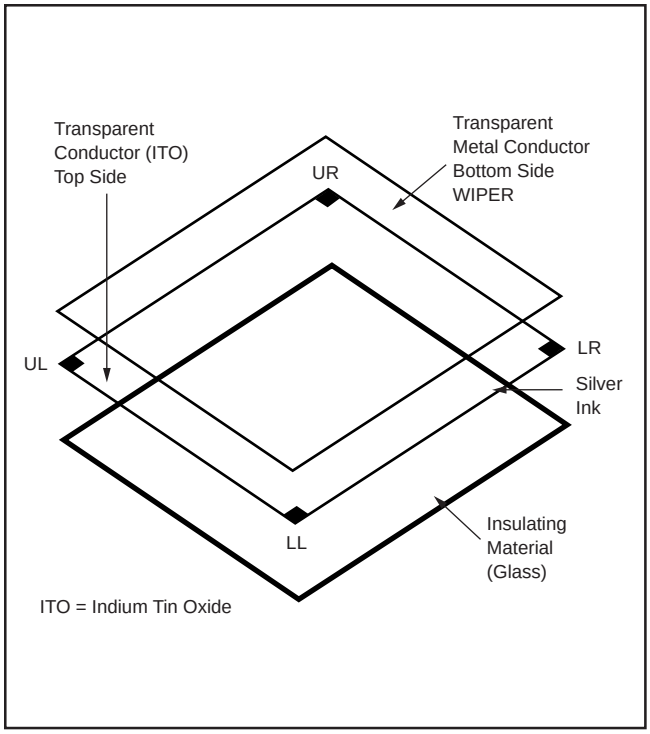

FIGURE 3. 5-Wire Touch Screen Construction.

DIFFERENTIAL vs SINGLE-ENDED MODE

The accuracy and reliability of conversions depend upon the ability of the converter to compensate for continuously varying operating conditions. These changing conditions have an effect on the voltages representing the X and Y coordinates. For example, if the A/D converter is configured for an absolute voltage reading (single-ended mode), changes in driver voltage drops will cause a misinterpreted input reading. However, if the A/D converter is configured in a ratiometric, or differential, mode, these errors can be virtually eliminated.

TOUCH SCREEN SETTLING TIME

When the touch panel is pressed or touched, there are two mechanisms that will affect the voltage level at the contact point of the touch panel. These two mechanisms will cause the voltage across the touch panel to "ring" (oscillate), and then slowly settle (decay) down to a stable DC value.

The two mechanisms are:

1) Mechanical bouncing caused by vibration of the top layer sheet of the touch panel when the panel is pressed.
2) Electrical ringing due to parasitic capacitance between the top and bottom layer sheets of the touch panel and at the input of ADS7843 that causes the voltage to "ring" (oscillate).

Single-Ended Mode

In single-ended mode, when a touch on the touch panel is detected, the processor that controls the ADS7843 will send a control byte to instruct the ADS7843 to perform a conversion. The ADS7843 then begins supplying voltage through the internal FET switches to the panel at the beginning of the acquisition period causing the voltage at the pressed point to rise. This rising voltage will "ring" as described above for a period of time before it finally settles to a stable voltage. After the acquisition period, all internal FET switches will turn off and the A/D converter will go into a conversion period. If the next control byte does not come during the current conversion period, the ADS7843 will go into power down or wait for the next instruction. With large capacitance across the panel, typically for filtering noise, caution should be exercised to insure that the corresponding input voltage for the X-position or Y-position coordinate pair has settled. In the single-ended mode, the input voltage must be settled during the last three clock cycles of the Data In word, or errors will occur.

Differential Mode

The operation of differential mode is similar to single-ended mode except that the internal FET switches will continue to be ON from the start of the acquisition period to the end of the conversion period. The voltage across the panel will also become the reference voltage to the A/D converter, providing a ratiometric operation. This means that if the voltage across the panel varies because of power supply changes, changes in the driver impedance with supply changes or temperature, or variations in the touch panel resistance with temperature these changes will be compensated for by the ratiometric operation of the A/D Converter.

However, if the selected channel of the next control byte to the ADS7843 is the same as the previous control byte and it comes during the current conversion period, the switches will not turn OFF after completing the current conversion. This will allow the input voltage to have a longer settling time and the settled voltage can be captured by the next control byte.

Difference Between Differential Mode and Single-Ended Mode

In both single-ended and differential modes, the ADS7843 acquires (samples) the input analog voltage from the touch panel for only three clock cycles (shown as t_{ACQ} in Figure 4). Hence, the input voltage has to settle within t_{ACQ} in order for the ADS7843 to capture the correct voltage.

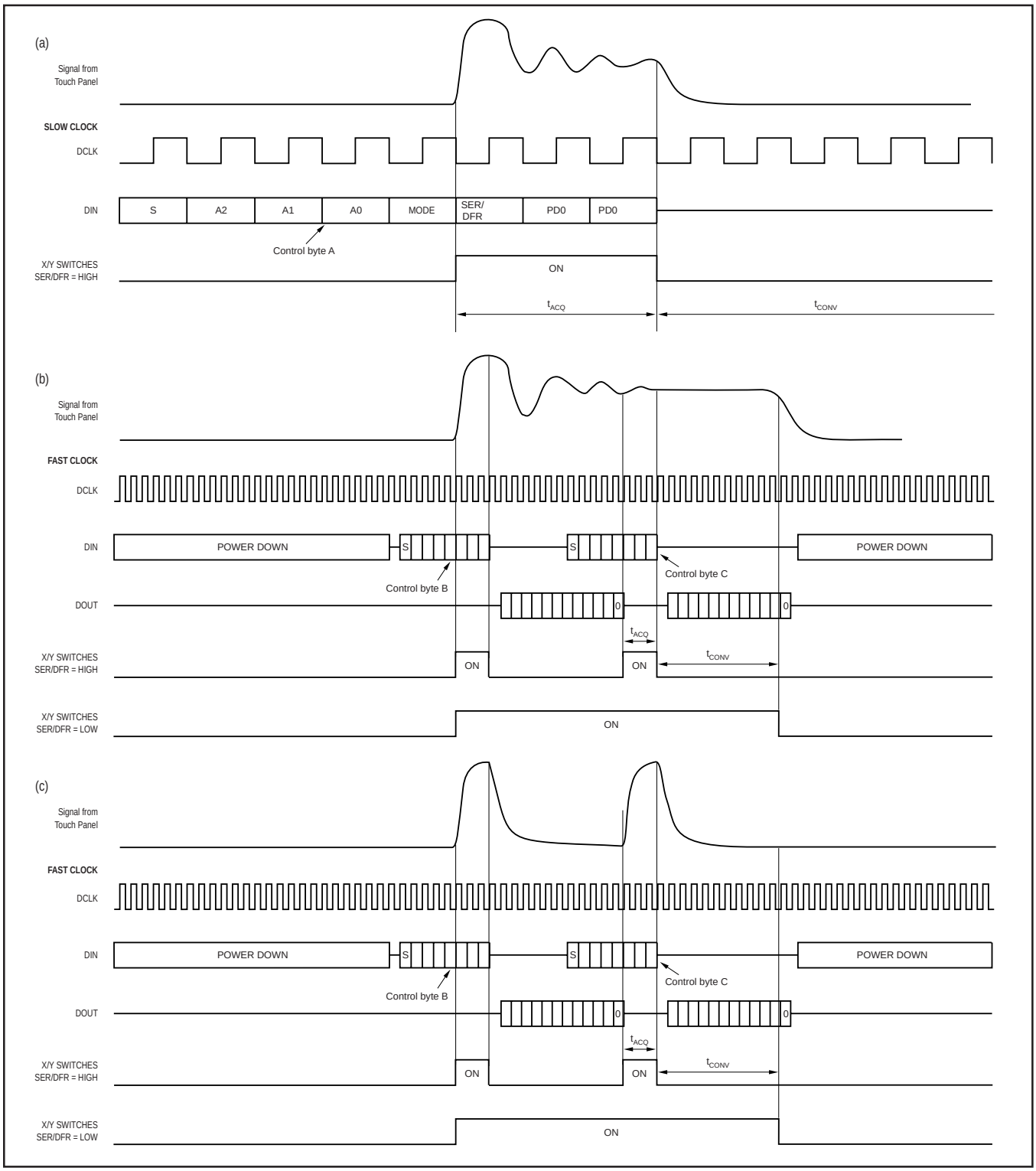

FIGURE 4. Timing Diagram of Differential and Single-ended Mode Operation for ADS7843.

Turning the drivers on causes the touch panel's voltage to rise rapidly, then settle to the final value, as shown in Figure 4. In order to acquire the correct value for conversion, the acquisition must be complete when the touch panel has completely settled. There are two ways of accomplishing this.

One method is shown in Figure 4 (a), using the ADS7843 in single-ended mode, and using a relatively slow clock. A slow clock extends the acquisition time, since it extends the three clock periods for acquisition. The drivers turn on at the beginning of the first of these three clock periods, and the panel must then settle completely during the following two clock cycles, so that at the end of the third clock cycle, the acquired voltage is accurate.

The second method, shown in Figure 4 (b), uses the differential mode and a much faster clock rate. Control Byte B turns the drivers on, and as before, the touch panel's voltage rises rapidly, and begins to settle. In this case, a conversion is done, and then a second conversion is begun, by send Control Byte C. If Control Bytes B and C are the same, the internal X/Y switch of the ADS7843 will not turn off after completing a conversion for Control Byte B. Thus, the touch panel voltage will be settled by the time the conversion from Control Byte C begins, and this conversion will be accurate. This method requires that the conversion result from Control Byte B be discarded, as it will not be accurate since its acquisition period occurred at the time that the touch panel voltage was still ringing.

Another advantage to using the second method is the potential for power savings. Figure 4 shows that the conversion period for Control Byte C (using the fast clock) ends before the conversion period for Control Byte A (using the slow clock). After the end of conversion for Control Byte C, the ADS7843 can go into power down mode and wait for the next sampling period. For the slow clock case, with Control Byte A, the next sample period may have to come immediately after the current conversion, leaving no time for power down.

Using a fast clock in single-ended mode would not be of any help, because as shown in Figure 4 (c), the drivers turn off between conversions. This results in the touch panel's voltage rising at the beginning of each conversion—the touch panel will never have a chance to settle in this case.

ADVANTAGES OF DIFFERENTIAL MODE OPERATION

- Able to handle touch panel with long settling time without extending acquisition time of the A/D converter.

  Figure 4 shows that if control byte B and C are the same, the internal X/Y switch of the ADS7843 will not turn off after completing a conversion for control byte B. This will provide enough time for the touch panel voltage to settle to a stable voltage.

  The converted data for control byte B will not be correct as its acquisition period occurred at the time that the touch panel voltage was still ringing. However, the converted data for control byte C will be correct because at the time of acquisition the touch panel voltage had already settled to a stable voltage.

- By using a faster clock, the ADS7843 will have some spare time to go into power down mode and hence conserve battery energy.

  Figure 4 shows that the conversion period for control byte C (fast clock) ends before the conversion period for control byte A (slow clock). After the end of conversion for control byte C, the ADS7843 can go into power down mode and wait for the next sampling period. However, for control byte A, the next sample period may have to come immediately after the current conversion, and hence no time for power down.

NOISY ENVIRONMENTS

Great care is needed in touch screen applications to prevent a noisy environment from detracting from the high performance of the measurement system. A touch screen on the input of a high impedance A/D converter is just like adding an antenna to the input of the system. The touch screen can pick up noise signals from the back-light source for the LCD display or from external EMI/RFI sources. The simplest way to minimize these noise sources is by adding capacitors from the touch screen drivers to ground, forming a low-pass filter. A typical value to start with is 0.01µF capacitors from each input/output to ground. Figure 5 shows the range of choices for filter capacitors, depending upon the touch panel plate resistance and desired number of coordinate-pair readings per second.

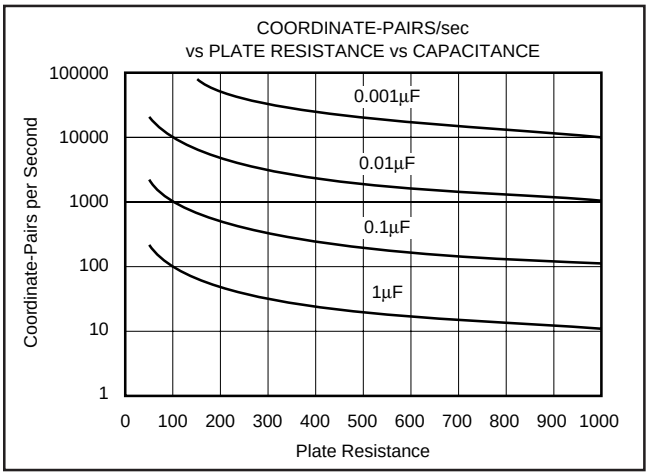

FIGURE 5. Filter Capacitor Selection Depends Upon Plate Resistance and the Number of Coordinate-Pair Readings per Second Desired.

The worst thing you can do is to put a series resistor in the lines from the driver to form a low-pass filter on the input. A series resistor will limit and lower the resolution of the converter because of the added voltage drop across the resistor. This drop could be significant depending upon the impedance of the touch screen used.

One issue to be aware of when adding capacitors for filtering is the effect they have on settling time of the touch-screen when the drivers are turned on. Depending on the A/D data rate and the mode of operation, the touch screen could never

settle to accurate levels, especially if operated in the single-ended mode. In the differential mode the touch-screen is connected during both acquisition and measurement mode and unless commanded to the power-down mode will continue to be connected through the drivers. Although it also relies on 3 clock cycles to acquire the input to the A/D, the touch-screen will eventually settle; keeping the power applied to the drivers over multiple measurements allows for a longer settling time. Depending on the time constant set by the touch-screen impedance and the filter capacitor necessary to reduce the noise to an acceptable level, several conversions may be required.

Several options are open for obtaining accurate results. The first alternative is to stretch the acquisition period, clocks 6, 7, and 8, by slowing the clock down during this time to achieve the necessary time delay for settling. By determining the time constant and allowing 9 time constants for 12-bit settling time, this will assure the touch-screen has settled. This can be done only during clock 6, 7, and 8, or can be done through the entire process. The minimum clock frequency to insure there is no droop in the sample-hold during the mearsurement cycle is 10kHz. The second alternative is to provide digital comparison of the measured voltage over several conversions and accept the reading when 2 or more consecutive readings are within acceptable limits, such as 2 or 3 counts.

In some applications, the noise levels can be very large and further filtering will be required to obtain stable readings. Utilizing an L/C pie filter on each of the four input/output lines can be used to achieve this level of filtering.

THE PEN INTERRUPT

The function of the pen interrupt pin is frequently misunderstood. This section serves to give more detailed information on the function of PENIRQ, and touches on the aspect of offset error that is introduced by the internal diode at the PENIRQ pin. Preventing false triggering of the PENIRQ is also explored .

OPERATION OF PENIRQ

The pen Interrupt feature of ADS7843 is implemented with a simple analog circuit; an open anode built-in diode.

By simply pulling-up the PENIRQ pin of ADS7843 to V_{CC}, a basic interrupt function can be implemented. Figure 6 shows the simplified schematic with the ADS7843 set to power down mode and pen interrupt enabled (PD1, PD0 = 00).

While the touch panel is untouched, the internal diode of the ADS7843 is not biased, and no current (or negligible leakage current) will flow. The voltage level at point A will be approximately V_{CC}.

When the touch panel is pressed, the internal diode of ADS7843 is forward biased and current flows to complete this current loop to ground (refer to current path of I_F in Figure 6). Now, the voltage at point A is pulled LOW to about one forward voltage drop of the diode. The LOW going voltage level a point A will signal the processor that

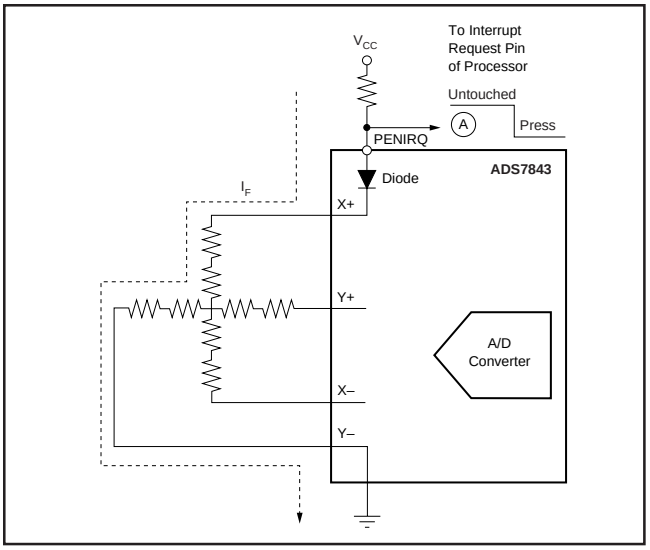

FIGURE 6. Simplified Schematic of ADS7843 for PD0, PD1 = 00.

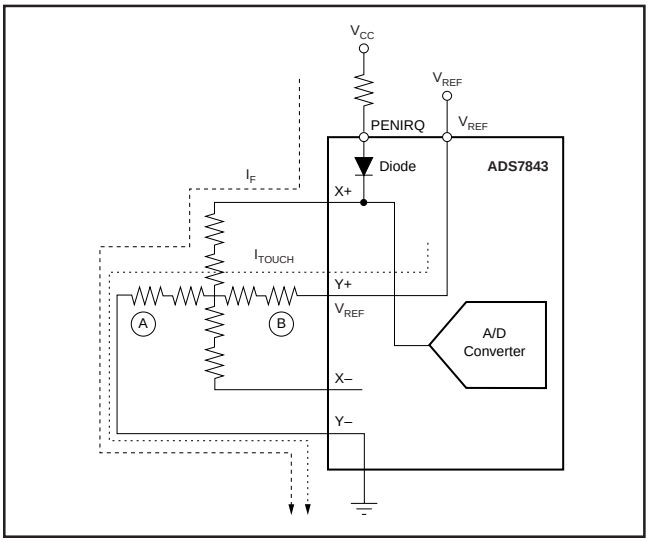

FIGURE 7. Simplified Schematic of ADS7843 for A2A1A0 = 001.

the panel is pressed. The processor will then execute its interrupt service routine to instruct the ADS7843 to perform a conversion.

The simple pull-up method shown in Figures 6 and 7 will introduce error to the A/D conversion. This error is often called offset error as it is caused by a DC leakage current through the internal diode (refer to the I_F current path in Figure 7). The current raises the voltage potential at the input of the A/D converter and creates a conversion error. This error is only introduced at Y-axis conversion because in X-axis conversion the internal diode is reversed biased.

Figure 7 shows the simplified schematic with the ADS7843 configured for Y-axis conversion (A2A1A0 = 001).

There are two current paths (labeled as I_F and I_{TOUCH} in Figure 7) through the touch panel when the panel is pressed. The I_{TOUCH} is the necessary current that develops voltage potential across the pressed point, whereas I_F is the unwanted current through the diode that causes an offset error in the conversion.

The current I_F is not constant throughout all locations on the touch panel. If the pressed point is near location A (see Figure 7), the diode will be heavily forward biased and I_F will be large, and hence offset error is large. However, if the pressed point is near location B, the diode will be turned off by the V_{REF}, I_F will be small (negligible) and so will the offset error.

Different I_F at different pressed points on the touch panel make this offset error difficult to compensate in software.

Solution For Offset Error

Figure 8 shows a recommended solution to minimize this offset error.

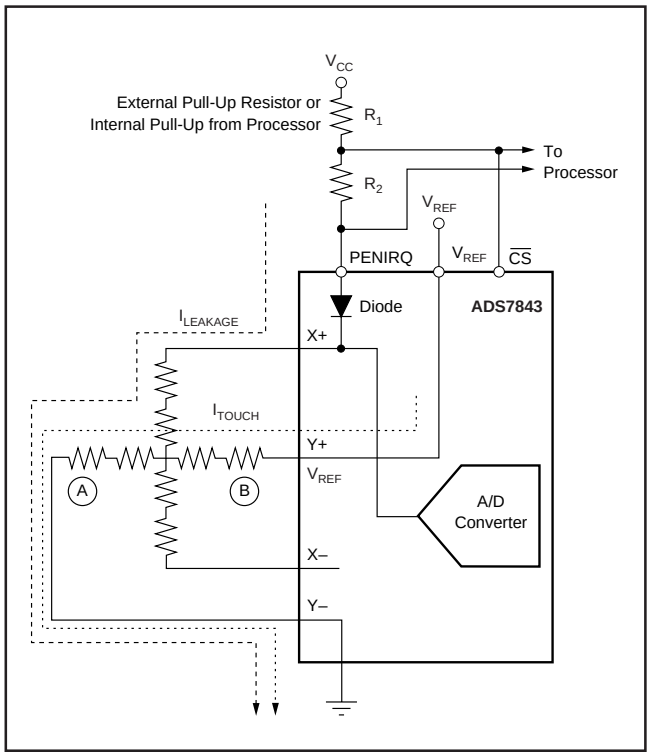

FIGURE 8. Recommended Solution to Minimize Offset Error.

In this solution, the PENIRQ pin is pulled-up with a resistor to the $\overline{CS}$ pin instead of V_{CC} supply as in Figure 7. When the $\overline{CS}$ pin is pulled LOW to activate the ADS7843, this low voltage will reverse bias the internal diode, or the diode is biased with very low forward voltage (depends on the contact point when the panel is pressed). Hence, only negligible leakage current will flow through the touch panel when the ADS7843 is activated.

The values of pull up resistors, R_1 and R_2, have to be carefully chosen such that:

1) If PENIRQ is pulled LOW by a touch on the touch panel, the voltage level at $\overline{CS}$ pin should not drop too low such that it will activate the ADS7843.

   This allows sharing of the serial bus and prevents noise from being coupled at the DIN input to be interpreted as a control byte.

   Since the ADS7843 is activated when the voltage at the $\overline{CS}$ pin goes below 0.8V, R_1 and R_2 have to be selected such that, in the worst case, the voltage at the $\overline{CS}$ pin is still above 0.8V. A typical value for R_2 is 20kΩ.

$$\frac{R_2}{R_1 + R_2}\left(V_{CC} - V_{DIODE}\right) - V_{DIODE} > 0.8V$$

$$R_2 > \frac{R_1}{11} \qquad \text{where } V_{DIODE} = 0.6V$$

2) The value of R_2 should be kept small enough to minimize the falling time (or response time) of the voltage level at PENIRQ when the panel is touched. Some processors are unable to detect a slow falling edge as an interrupt.

The pen interrupt circuit on the ADS7845 and ADS7846 is implemented differently than it is on the ADS7843. On the ADS7845 and ADS7846, during the measurement cycles for X– and Y-Position, the PENIRQ output diode will be internally connected to GND and the X+ input disconnected from the PENIRQ diode to eliminate any leakage current from the pull-up resistor to flow through the touch screen, thus causing no error.

False Triggering

Noise on the X+ input can cause false triggering of a touch to the touch-screen due to its connection to the Pen Interrupt output. An R/C filter on this output, such as a 1Ω resistor and 0.01µF capacitor to ground, can be used to filter noise spikes to ground and help prevent false touches.

INPUT PROTECTION FOR ADS7843

Figure 9 gives some recommendations to protect the ADS7843 from failure due to high energy spikes being coupled into the device from the touch screen. These spikes may be the result of ESD, or may come from a backlight power supply. Adding ferrite beads and clamping diodes on the touch panel's X and Y lines will help dissipate this type of energy before it reaches the ADS78343, and prevent damage to the part should the amplitude of these spikes exceed the supply voltage.

SOFTWARE EXAMPLES FOR DIFFERENTIAL MODE

This section gives two software examples with some ideas on controlling the ADS7843 to operate in the differential mode.

Figures 10 and 11 show the algorithm of two software examples to interface a processor with the ADS7843. The two software examples assume that the ADS7843 is configured to operate in differential mode with 16 clocks-per-conversion protocol (see Figure 6 in the ADS7843 data sheet). The software will return the X-axis coordinate conversion result as DATA X and the Y-axis conversion result as DATA Y.

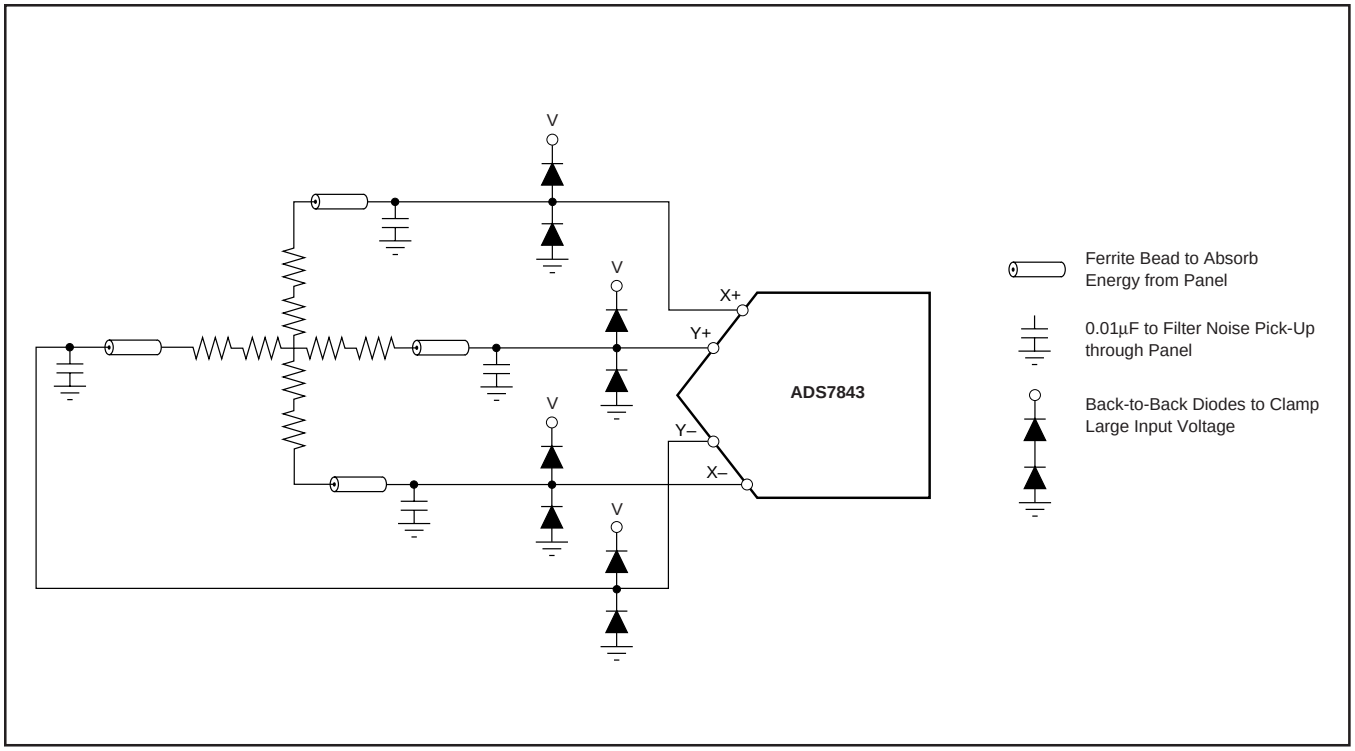

FIGURE 9. Input Protection for ADS7843.

Flowchart 1

Figure 10 shows an example of using the software de-bouncing method to overcome touch panel signal ringing for both an interrupt signal and conversion.

In this solution, DATA1 is used to store current conversion results, DATA2 is used to store previous conversion results, and DATA X and DATA Y are used to store valid X-axis and Y-axis conversion results, respectively. DATA1 and DATA2 are used together to realize S/W de-bouncing that confirms the conversion result is valid when the current and previous conversion results are the same. This provides a flexible approach for the software to handle touch panels of different settling characteristics. It is, however, prone to misinterpretation of valid conversions when the ringing frequency of the input voltage is very close to the sampling rate.

Flowchart 2

Figure 11 is another example that uses the software de-bouncing solution to overcome signal ringing problems for the interrupt signal, and takes the last (n^{th}) conversion result as the valid conversion.

This solution is much simpler than the previous one, but is only suitable for touch panels that have similar settling characteristics. It takes the last conversion result as a valid conversion result instead of using S/W de-bouncing method. The value of “n” is dependent on the settling time of the input voltage to the ADS7843. The user has to test out a number of touch panels before deciding on the value of “n”.

NOTE: If you need to put the ADS7843 into power-down mode with PENIRQ enabled, you will need to execute an additional conversion cycle with PD1 and PD0 set to ‘00’. However, if the 15-Clock conversion cycle mode is used, you can set PD1 and PD0 as ‘00’ for both X and Y-axis conversion.

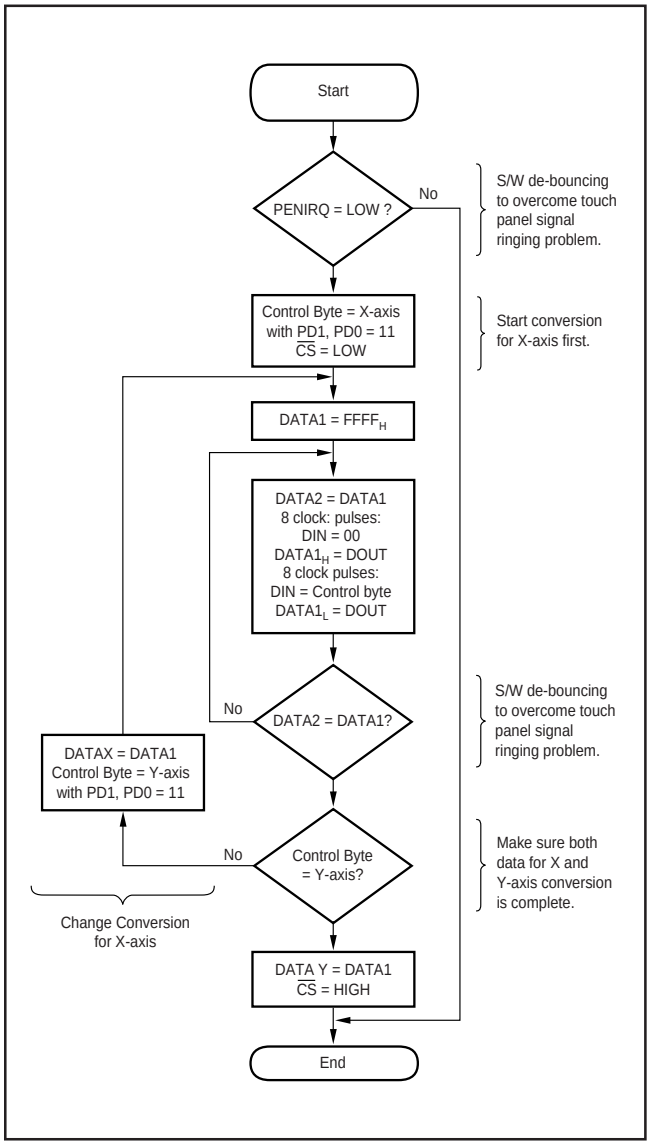

FIGURE 10.

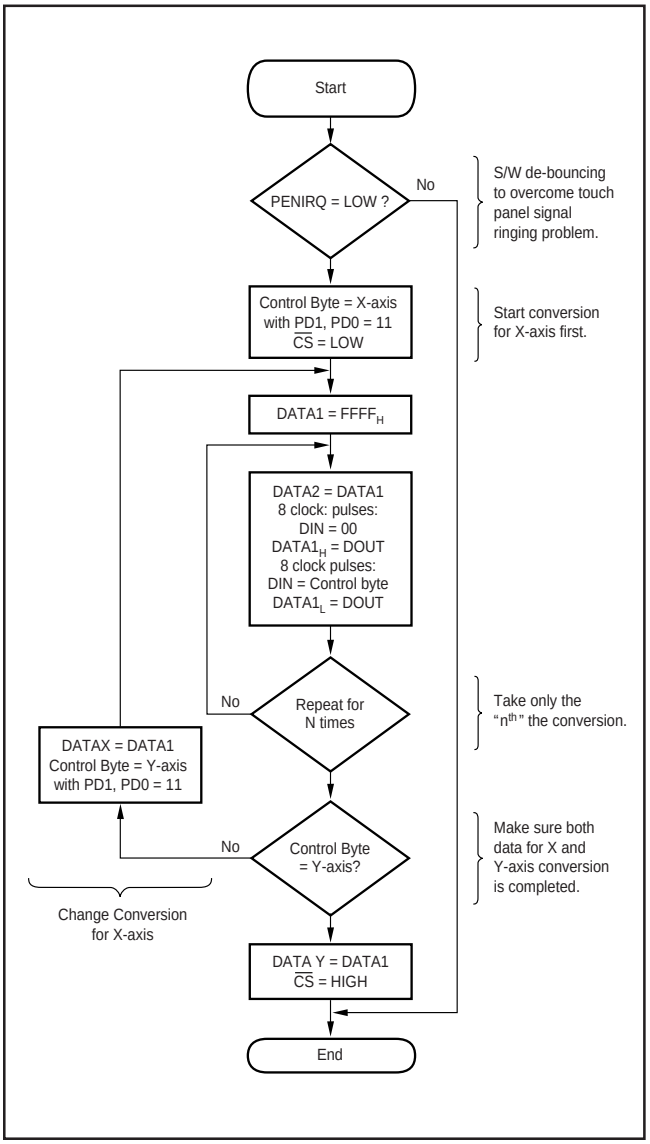

FIGURE 11.

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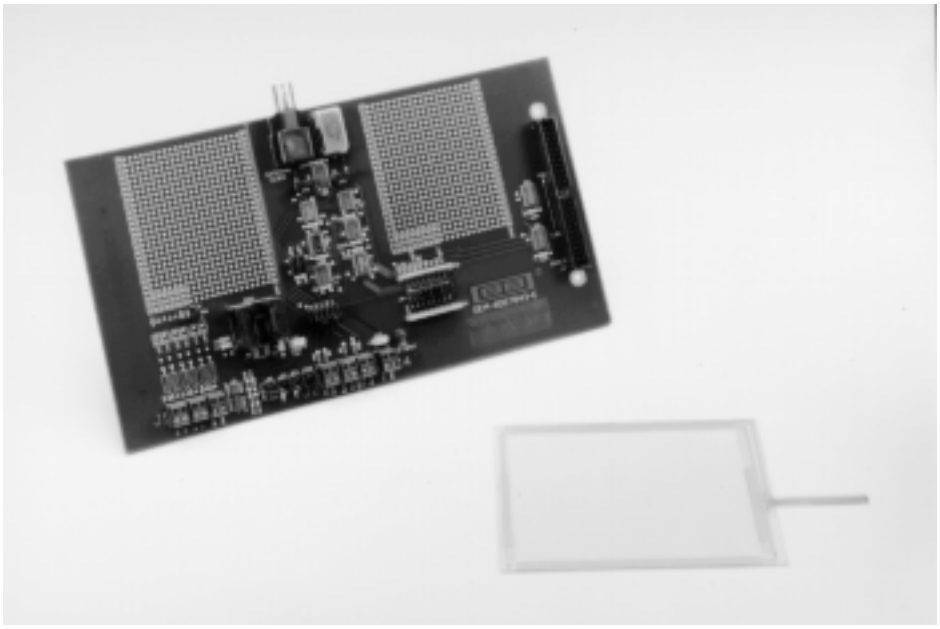
DEM-ADS7843E/45E

EVALUATION FIXTURE



FEATURES

- STAND-ALONE CAPABILITY
- FLEXIBLE CLOCK PROGRAMMING
- USER-CONFIGURABLE A/D CONVERTER OPERATION
- ANALOG BREADBOARD AREA
- DIGITAL BREADBOARD AREA
- FLEXIBLE REFERENCE VOLTAGE PROGRAMMING

APPLICATIONS

- DATA ACQUISTION
- PERSONAL DIGITAL ASSISTANTS
- 4- OR 5-WIRE RESISTIVE TOUCH SCREEN
- PORTABLE INSTRUMENTS

DESCRIPTION

The DEM-ADS7843E/45E evaluation fixture is designed for quick evaluation of Burr-Brown's ADS7843E (4-wire) and ADS7845E (5-wire) touch-panel controllers. The board has features that allow the user to evaluate all the functions of the analog-to-digital converter. The options offered to the user include a flexible clock generator circuit, an analog breadboard area, a digital breadboard area, and an easily-configurable voltage reference. The DEM-ADS7843E/45E has been designed to accommodate stand-alone operation, allowing the user to easily connect directly to 4-wire (ADS7843E) or 5-wire (ADS7845E) touch-screen panels and to an external processor. This evaluation fixture has a quick-release socket for easy evaluation of mulitiple converters or a solder footprint to allow the user to solder the DUT directly to the board.

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INSTALLATION

The DEM-ADS7843E/45E evaluation fixture is designed for stand-alone evaluation or evaluation using the clocking network on the board. Stand-alone evaluations imply that the A/D converter is powered by J4 (power supply connector) and the user is put to the task to provide analog and digital input excitation. This is achieved by removing all five jumper tops of JP4 and using J1 and J2 for direct connections to the device under test (DUT).

In contrast, the DEM-ADS7843E/45E/45E board has the appropriate digital interface circuitry to drive the DUT data clock, chip select, and serial data in which is coordinated with the BUSY and PENIRQ to provide serial and parallel output data.

This kit includes the following items:

ADS7843E Evaluation Fixture—A2518

DEM-ADS7843E/45E Documentation (LI-522)

ADS7843E (5 samples)

ADS7845E (5 samples)

The DEM-ADS7843E evaluation fixture has two positions on the board for the A/D converter to be installed in. The first position is the socket, DUT1 on the board. This spring-loaded socket allows the user to quickly swap in or out the device that is being evaluated. The other option on the board is the position X1, which is a solder location for the DUT. If this option is chosen, the user must solder the DUT directly to the board. This position is only useful for 2 or 3 solder cycles.

CAUTION: DO NOT connect the a device into the DUT1 socket and have another device soldered to the board in position X1 at the same time.

The additional equipment required to do a complete evaluation of the performance of the ADS7843E or ADS7845E comprises of:

+5VDC power supply

Voltage or current signal source

4-Wire (ADS7843E) or 5-Wire (ADS7845E) Resistive Touch Screen

To install the DEM-ADS7843E/45E evaluation fixture, connect the appropriate power supply to J4. When power is applied to the DEM-ADS7843E/45E, the red LED on the board should light.

J1	Analog Input Interface. Each connector is labeled.
J2	Digital I/O Interface. Each connector is labeled.
J3	Parallel Output Port.
J4	Power Supply Connector. This connector powers the DUT and digital network. Refer to the ADS7843 or ADS7845 product data sheet for power supply restrictions. All digital chips on the DEM-ADS7843E/45E board are capable of operating with supply voltage from 2.7V to 5.25V.
P1	External DCLK Connector.

TABLE I. Connectors (Jx and P1) Assignments.

USER CONFIGURATIONS

The DEM-ADS7843E/45E evaluation fixture provides the right combination of jumper options and support circuitry to allow for a variety of evaluation configurations. Throughout this data sheet, numerous references are made to the ADS7843 and ADS7845 A/D converters. For more information concerning these devices, refer to the ADS7843 or ADS7845 data sheet. The circuit is laid out with a four-layer board. The two outside layers are for circuit traces and the inner layers are the ground and power planes. The analog and digital planes of the circuit is separated through the middle of the board all the way to the power supply connector, where they are joined. The circuit diagram and layout diagrams for the DEM-ADS7843E/45E is shown in Figure 1 and Figures 4 through 7.

JUMPER NUMBER	FACTORY SETTING	DESCRIPTION
JP1	B	Voltage reference. This setting connects A/D converter reference to $+V_{CC}$.
JP2, JP11, JP10	JP2 = Not Installed JP11 = Not Installed JP10 = Not Installed	Inverted or non-inverted option for PENIRQ of the ADS7843 or ADS7845 when driving this pin through pin 2. This setting sets this pin HIGH and connects this pin to J2.
JP3	D, F, G	Hardwire digital jumpers for DIN serial code. This setting configures the A/D converter for S = HIGH, A2-A0 = 001, MODE = LOW, SGL/DIF = HIGH, PD1-PD0 = 11.
JP4	A, B, C, D, E	This jumper connects the clocking network to the DUT.
JP5, JP6	JP5 = A JP6 = B	Clock speed options. This configuration sets the board using Y1/10 as the DCLK frequency.
JP7, JP8	JP7 = B JP8 = A	Optional 16- or 24-bit operation. This configuration sets the board for 16 DCLK per conversion cycle.
JP9	B	Used to personalize the board for the ADS7843 or ADS7845. Position B = ADS7843 or ADS7845.

TABLE II. Jumper (JPx) Assignments.

DUT CONNECTIONS

The DEM-ADS7843E/45E DUT Board has a socket for the DUT which is positioned in the DUT1 position. Additionally, it has a solder footprint in the event that the user chooses to solder the DUT directly to the board. This footprint is poisitioned in X1, just below the DUT1 socket. If the solder footprint is used, care should be taken to preserve the solder pads for repeated soldering. Bad X1 solder pads do not interfere with the operation or connections of the DUT1 socket.

The DEM-ADS7843E/45E evaluation fixture is designed to evaluate both the ADS7843 and ADS7845 A/D converters. JP9 must be in position B to evaluate either the ADS7843 or ADS7845.

Space for an R/C input filter has been provided to allow user customization for the particular application. Shorting bars have been installed in R_3, R_5, R_7, R_9, R_{10}, and R_{12} positions on the board. These are positioned betwen the input of the DUT and the pin connector, P1. Shorting bars were used to allow for immediate evaluation of a four-wire touch screen. In this situation, the touch screen would provide the source resistance. If resistors are desired in positions R_3, R_5, R_7, R_9, R_{10}, and R_{12}, the user can solder in the desired values. Additionally, positions for capacitors at the input of the DUT are provided with C_3, C_4, C_5, C_6, C_9 and C_{10}. Once again, the user must install appropriate values for the application under evaluation.

The voltage reference to the DUT is programmed in the JP1. The JP1 options are given in Table III.

POSITION	RESULTING CONFIGURATION
A	1.2V is configured to pin 9 (V_{REF}) of the DUT.
B	The power supply from J4 is configured to pin 9 (V_{REF}) of the DUT.
C	2.5V is configured to pin 9 (V_{REF}) of the DUT.

TABLE III. V_{REF} is Programmed Using JP1 Position Options.

The combination of JP2 allows jumper programmable settings of the PENIRQ of the ADS7843 or ADS7845 pin of the DUT. Additionally, this pin can be accessed through J2 and a combination of JP10 and JP11. Refer to Table IV for jumper position details. Refer to the ADS7845 data sheet for additional options.

The digital I/O pins of the DUT may be driven or monitored with the J2 connector. The assignment of these pins are summarized in Table V.

J2 PIN NUMBER (From Left to Right)	ADS7843 PIN DESCRIPTION
1	$\overline{CS}$
2	DCLK
3	BUSY
4	DIN
5	PENIRQ
6	DOUT

TABLE V. J2 Connector Contacts versus DUT Pins. (NOTE: If you have a DEM-ADS7843E/45E, Revision A, the silkscreen is in error. The above description is correct.)

STAND-ALONE OPERATION

The DUT can be evaluated in a stand-alone configuration by removing all of the jumper tops of JP4. JP4 connects pins 12, 13, 14, 15, and 16 of the DUT to the digital interface circuitry of the board. If the array of jumper tops are not removed, the user may find significant conflicts on the digital I/O lines of the DUT. The details of this interface circuitry is discussed in detail in the “Digital Interface” section of this data sheet.

DIGITAL INTERFACE CIRCUITRY

The DUT can be evaluated using the digital clocking circuitry on the board by installing all of the jumper tops of JP4 and removing any signal present on the J2 connector. This digital circuit uses the clock signal from P1 (External Clock) or Y1 to create the DUT clock (DCLK), CS, and the DIN code to the device while providing a serial or parallel output signal from the DOUT pin of the DUT.

Clock Control

The master clock to the board is set with the JP6 jumper. Position A of the JP6 jumper configures the External Clock (P1) coax connector into the circuit. It is recommended that this signal be a logic square wave. The signal from this connector will be used directly for the DCLK signal to the

JP2 POSITION	JP10 POSITION	JP11 POSITION	RESULTING CONFIGURATION
Not Installed	Not Installed	Not Installed	Pin 11 of the DUT is HIGH.
Not Installed	Installed	Not Installed	Pin 11 of the DUT is connected to position 5 of J2. If there is no connection to position 5 of J2, pin 11 of the DUT will default HIGH.
Not Installed	Not Installed	Installed	Pin 11 of the DUT is inverted and connected to position 5 of J2. If there is no connection to position 5 of J2, pin 11 of the DUT will default HIGH.
Installed	Not Installed	Not Installed	Pin 11 of the DUT is LOW.
Installed	Installed	Not Installed	Pin 11 of the DUT is connected to position 5 of J2. If there is no connection to position 5 of J2, pin 11 of the DUT will default LOW.
Installed	Not Installed	Installed	Pin 11 of the DUT is inverted and connected to position 5 of J2. If there is no connection to position 5 of J2, pin 11 of the DUT will default LOW.

TABLE IV. PENIRQ (ADS7843 or ADS7845) Jumper Settings.

DUT. Refer to the ADS7843 or ADS7845 data sheet for the proper restrictions on this clock. Alternatively, a clock oscillator that is installed in Y1 can be used as the master clock. The signal from this device is either divided by 10 or divided by 20 per JP5. The settings from JP5 are listed in Table VI.

JUMPER SETTING	RESULTING CONFIGURATION
A	Y1 Frequency divided by 10. In conjunction with JP6 = B, this frequency becomes DCLK for the DUT.
B	Y1 frequency divided by 20. In conjunction with JP6 = B, this frequency becomes DCLK for the DUT.

TABLE VI. Jumper Settings for Using Y1 as Master Clock.

Clocks per Conversion Control

Once DCLK is set (per clock control instructions) the conversion cycle of the DUT can be configured to either take 16 or 24 clock cycles. The jumper configuration for these two modes of operation are shown in Table VII. Additionally, the timing diagram of these two modes of operation are shown in Figures 2 and 3.

JP7	JP8	RESULTING CONFIGURATION
A	B	24 DCLK cycles per conversion
B	A	16 DCLK cycles per conversion

TABLE VII. The Digital Support Circuitry Can be Operated in a 16 Clocks per Conversion or a 24 Clocks per Conversion with the Jumper Settings Described in the Table. Refer to Figures 2 and 3 for specific timing.

DIN Programming

The DIN input (DUT, pin 14) receives an 8-bit serial input data stream which programs the ADS7843 or ADS7845 X or Y input channel, mode and power-down options. This serial stream can be programmed with JP3. JP3 is essentailly an 8-bit parallel configuration which is processed by a parallel-to-serial converter (U8) and then transmitted to the DUT at the appropriate time. Even when a position on JP3 is jumper top configured, digital gates can over drive their settings. Consequently, these lines are also connected to the digital breadboard area, which gives the user more flexibility in terms of programming this serial command byte.

Parallel Output

The combination of U13 and U14 converts the digital output of the DUT into a parallel word. This parallel word appears on the connector J3. A DVALID trigger is also provided on J3. Refer to Table VIII for the J3 connector configuration.

J3 PIN	DESCRIPTION
1	$\overline{\text{DVALID}}$
11	LSB
13	LSB + 1
15	LSB + 2
17	LSB + 3
19	LSB + 4
21	LSB + 5
23	LSB + 6
25	LSB + 7
27	LSB + 8
29	LSB + 9
31	LSB + 10
33	MSB
3, 5, 7, 9	Digital LOW
35 through 50	Open
All Even Pins	GND

TABLE VIII. J3 Configuration.

PART LOCATION	NUMBER PER KIT	PART NUMBER	VENDOR	DESCRIPTION
	1	A-2518 Rev B		ADS7843E Bare Board
X1 (not installed)	1	Accepts ADS7843E and ADS7845E	Burr-Brown	12-bit A/D converter solder land area, parts not installed
U1	1	REF1004C-1.2	Burr-Brown	1.235V Reference, SOIC
U2	1	REF1004C-2.5	Burr-Brown	2.5V Reference, SOIC
DUT	5	ADS7843E	Burr-Brown	12-bit Touch Screen A/D Converter (4-wire panel)
DUT	5	ADS7845E	Burr-Brown	12-bit Touch Screen A/D Converter (5-wire panel)
DUT (socket)	1	OTS-16(24)-0.635-01	Enplas (TESCO)	16-lead SSOP socket
U3, U5, U7	3	74HC393D	TI(1)	Dual, 4-bit, binary counter
U4	1	74HC08D	TI(1)	Quadruple two-input positive AND gates
U6	1	74HC04D	TI(1)	Hex Inverters
U8	1	74HC166D	TI(1)	8-bit parallel-load shift register
U13, U14	2	SN74HC594D	TI(1)	8-bit shift registers with output registers
U15	1	MC74HC390D	TI(1)	Decade counter, dual 4-bit
Y1	1	CTX129-ND	DigiKey	32MHz clock oscillator, (CTS)
Y1 (socket)	1	1107741	Aries	14-pin oscillator socket, DIP
D1	1	HLMP-3201	Hewlett Packard(1)	Red LED
R_3, R_5, R_7, R_9, R_{10}, R_{12}				Optional. Provided with shorts. Resistors not included.
R_{13}	1	CRCW12062001F	Dale	2kΩ, 1%, 0.125W, metal-film resistor
R_{14}	1	CRCW12061001F	Dale	1kΩ, 1%, 0.125W, metal-film resistor
R_{15}, R_{16}	2	CRCW120622R1F	Dale	22.1kΩ, 1%, 0.125W, metal-film resistor
R_1, R_{11}	2	CRCW12061002F	Dale	10kΩ, 1%, 0.125W, metal-film resistor
R_8, R_{18}	2	CECW12061003F	Dale	100kΩ, 1%, 0.125W, metal-film resistor
R_2, R_4, R_6	3	CRCW12061000F	Dale	100Ω, 1%, 0.125W, metal-film resistor
R_{17}	1	CRCW12066810F	Dale	681Ω, 1%, 0.125W, metal-film resistor
C_1	1	T491B225K016AS	Kemet	2.2µF capacitor, 16V
C_3 through C_6, C_9, C_{10}				Optional. Capacitor not included.
C_{12}, C_{14} through C_{25}	13	C1206C104K5RAC	Kemet	0.1µF surface-mount capacitor, X7R
C_{11}, C_{13}	2	T491C106K016AS	Kemet	10µF polarized capacitors, 16V, 10%
C_2	1	C1206C103K5RAC	Kemet	0.01µF, 50V, 10%, chip-ceramic, X7R
C_8	1	C320C104K5R5CA	Kemet	0.1µF, 50V, 10%, ceramic
JP1	1	TSW-103-07-T-D	Samtec	2 x 3
JP2	1	TSW-101-07-T-D	Samtec	2 x 1
JP3	1	TSW-108-07-T-D	Samtec	2 x 8
JP4	1	TSW-105-07-T-D	Samtec	2 x 5
JP5 through JP9	5	TSW-103-07-T-S	Samtec	1 x 3
JP1, JP2, JP3 tops	3	SNT-100-BK-T	Samtec	Jumper Tops
J1, J2, J4 pins	7	31024102	RIACON	2-pin terminal block pins, 3.5mm centers
J1, J2, J4 tops	7	31165102	RIACON	2-pin terminal block tops, 3.5mm centers
J3	1	IDH-50LP-S3-TG	Robinson Nugent	2 x 25, straight-through header w/shroud, 0.1" center spacing
P1	1	47788	Pamona	BNC right-angle, PC mount connector
RN2	1	CSC10A-01-104F	Dale	10-pin SIP resistor network (100kΩ, 9R, 1C)
RN1	1	CSC10A-01-103F	Dale	10-pin SIP resistor network (10kΩ, 9R, 1C)
Rubber Feet	6	SJ5523-O-ND	3M	Bumpons

NOTE: (1) Or equivalent.

TABLE IX. Parts List for the DEM-ADS7843E/45E.

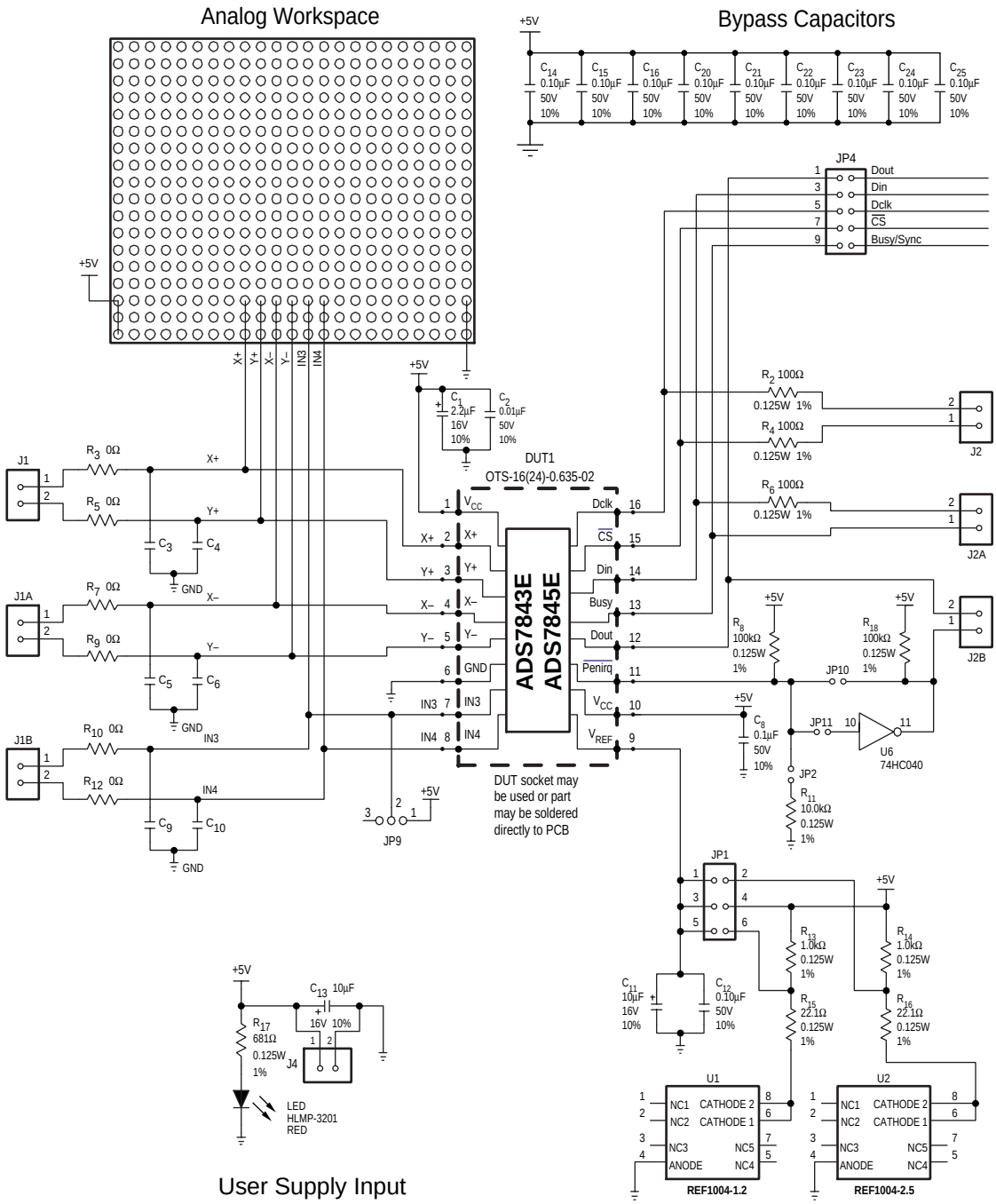
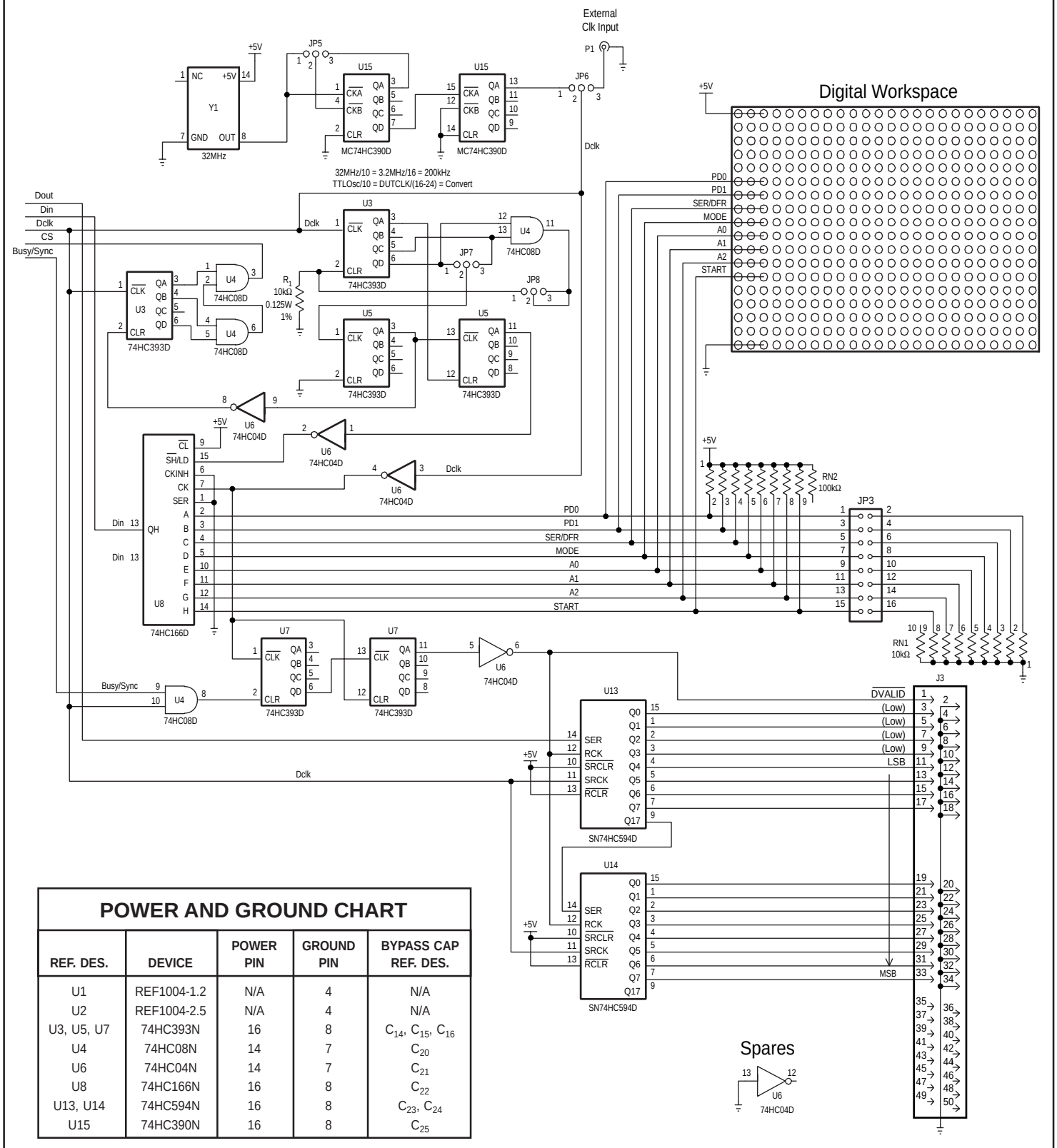


FIGURE 1a. ADS7843E and ADS7845E Evaluation Demo Board Analog Circuit Diagram.



POWER AND GROUND CHART

REF. DES.	DEVICE	POWER PIN	GROUND PIN	BYPASS CAP REF. DES.
U1	REF1004-1.2	N/A	4	N/A
U2	REF1004-2.5	N/A	4	N/A
U3, U5, U7	74HC393N	16	8	C_{14}, C_{15}, C_{16}
U4	74HC08N	14	7	C_{20}
U6	74HC04N	14	7	C_{21}
U8	74HC166N	16	8	C_{22}
U13, U14	74HC594N	16	8	C_{23}, C_{24}
U15	74HC390N	16	8	C_{25}

FIGURE 1b. ADS7843E and ADS7845E Evaluation Demo Board Digital Circuit Diagram.

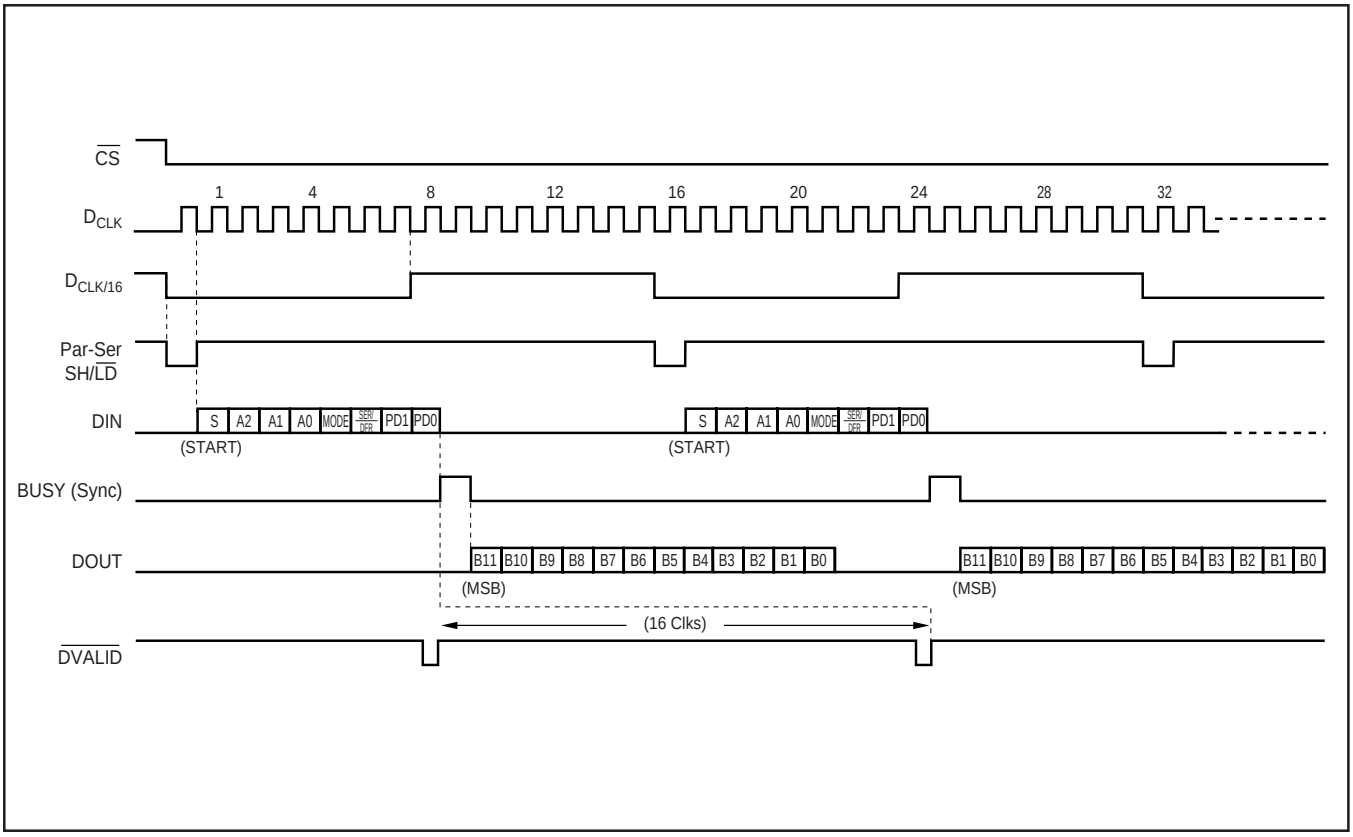


FIGURE 2. ADS7843E and ADS7845E Conversion Timing Diagram, 16 Clocks per Conversion.

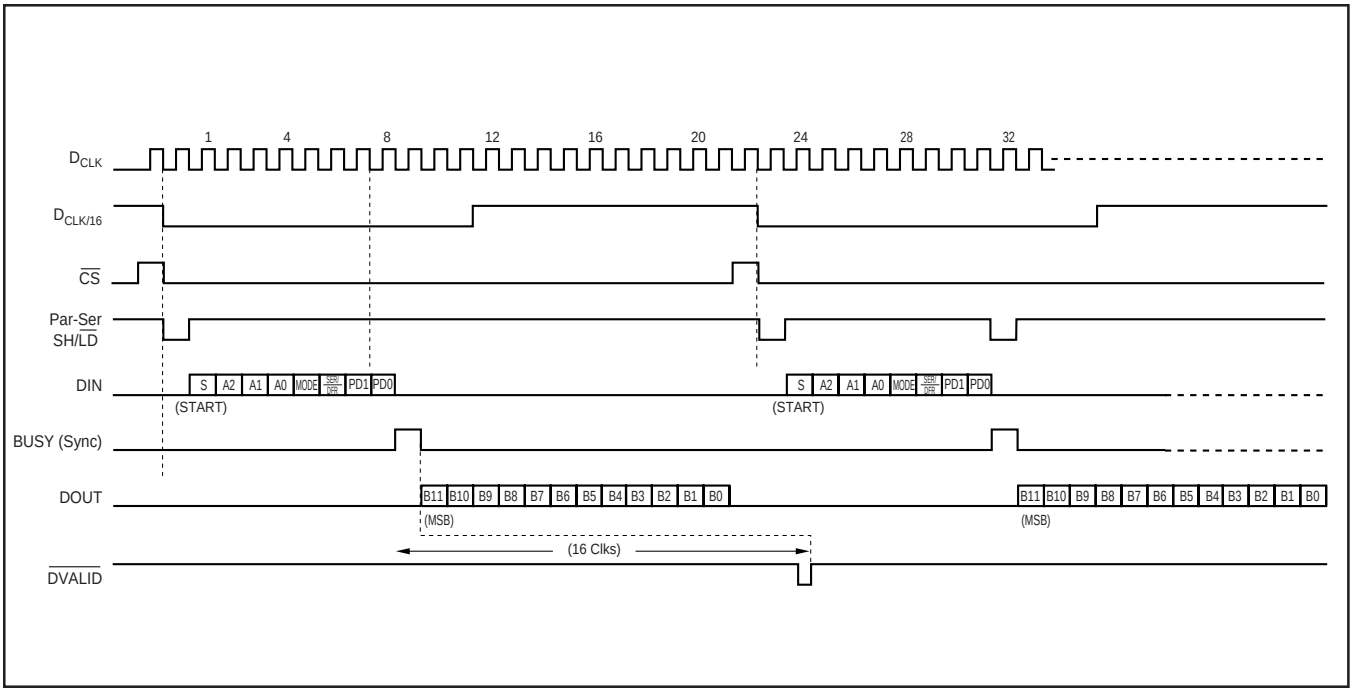


FIGURE 3. ADS7843E and ADS7845E Conversion Timing Diagram, 24 Clocks per Conversion.

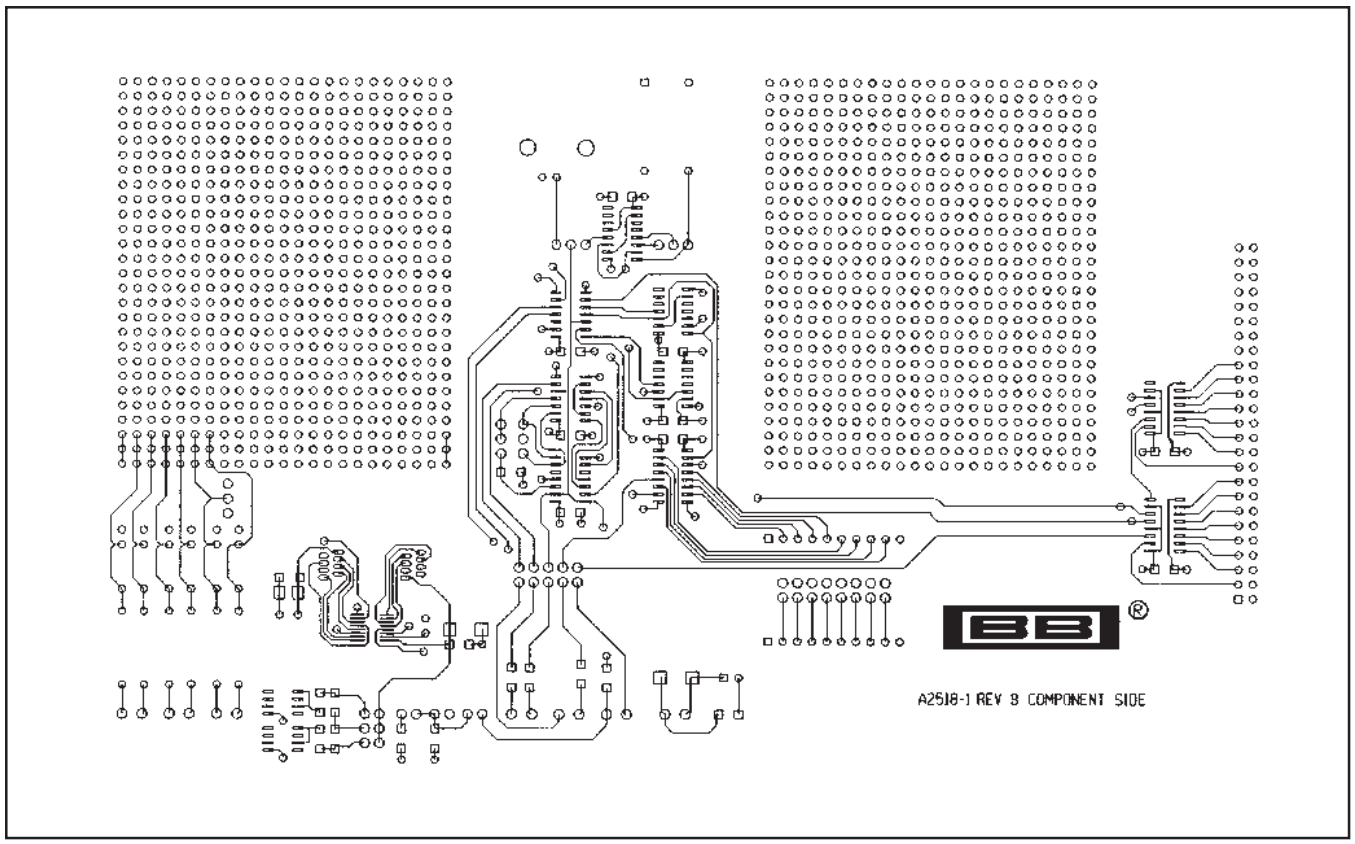


FIGURE 4. Component Side of the DEM-ADS7843E/45E Demonstration Board.

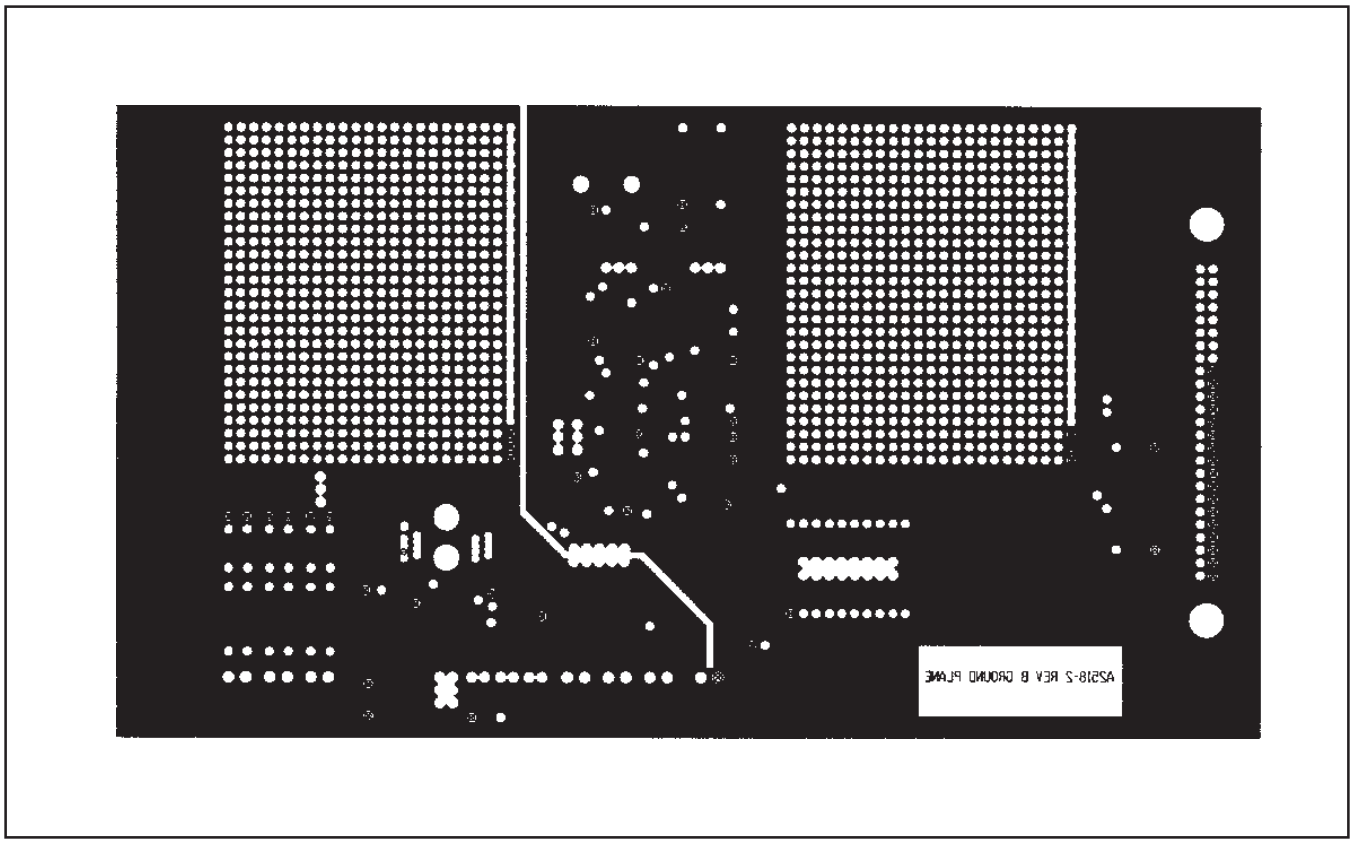


FIGURE 5. Ground Plane of the DEM-ADS7843E/45E Demonstration Board.

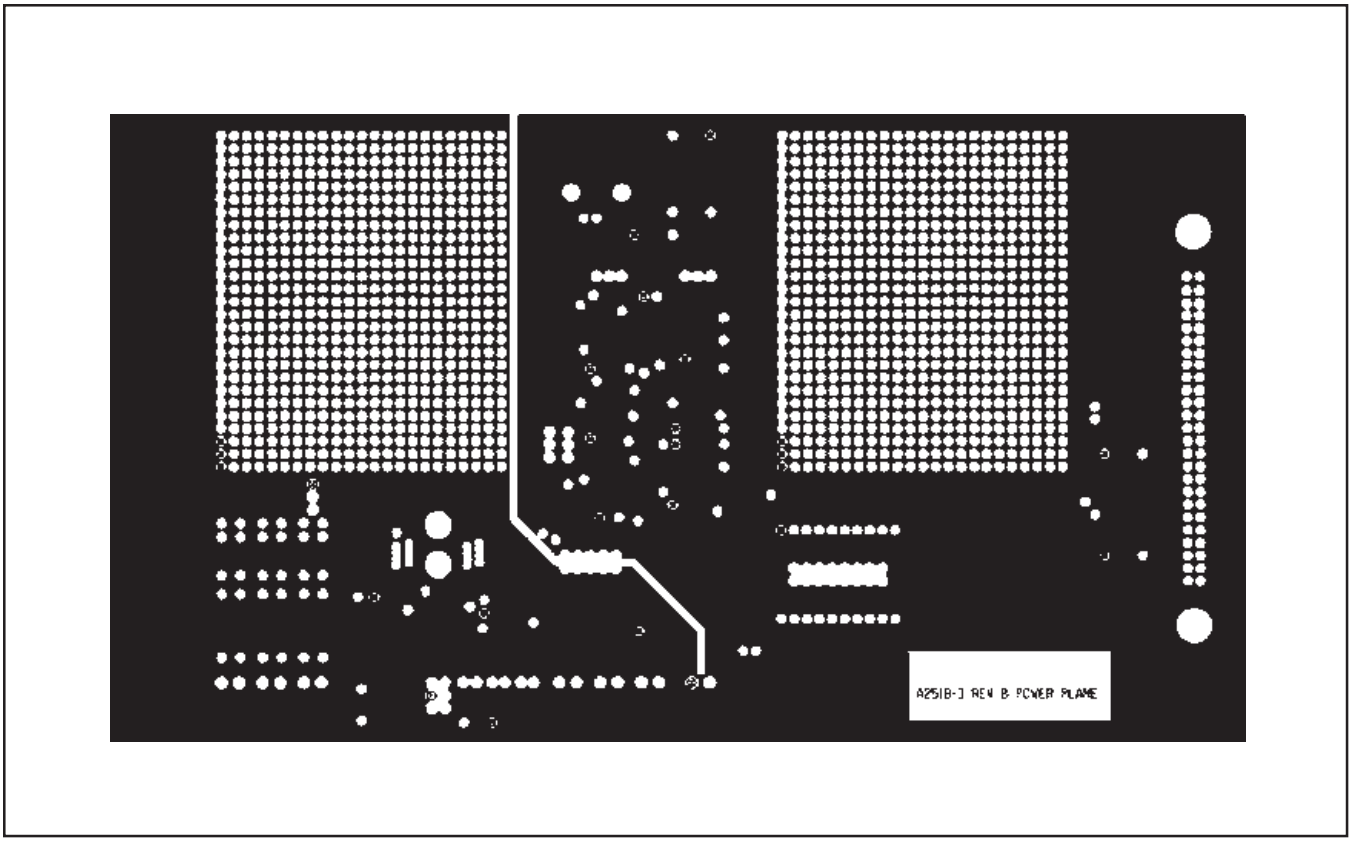


FIGURE 6. Power Plane of the DEM-ADS7843E/45E Demonstration Board.

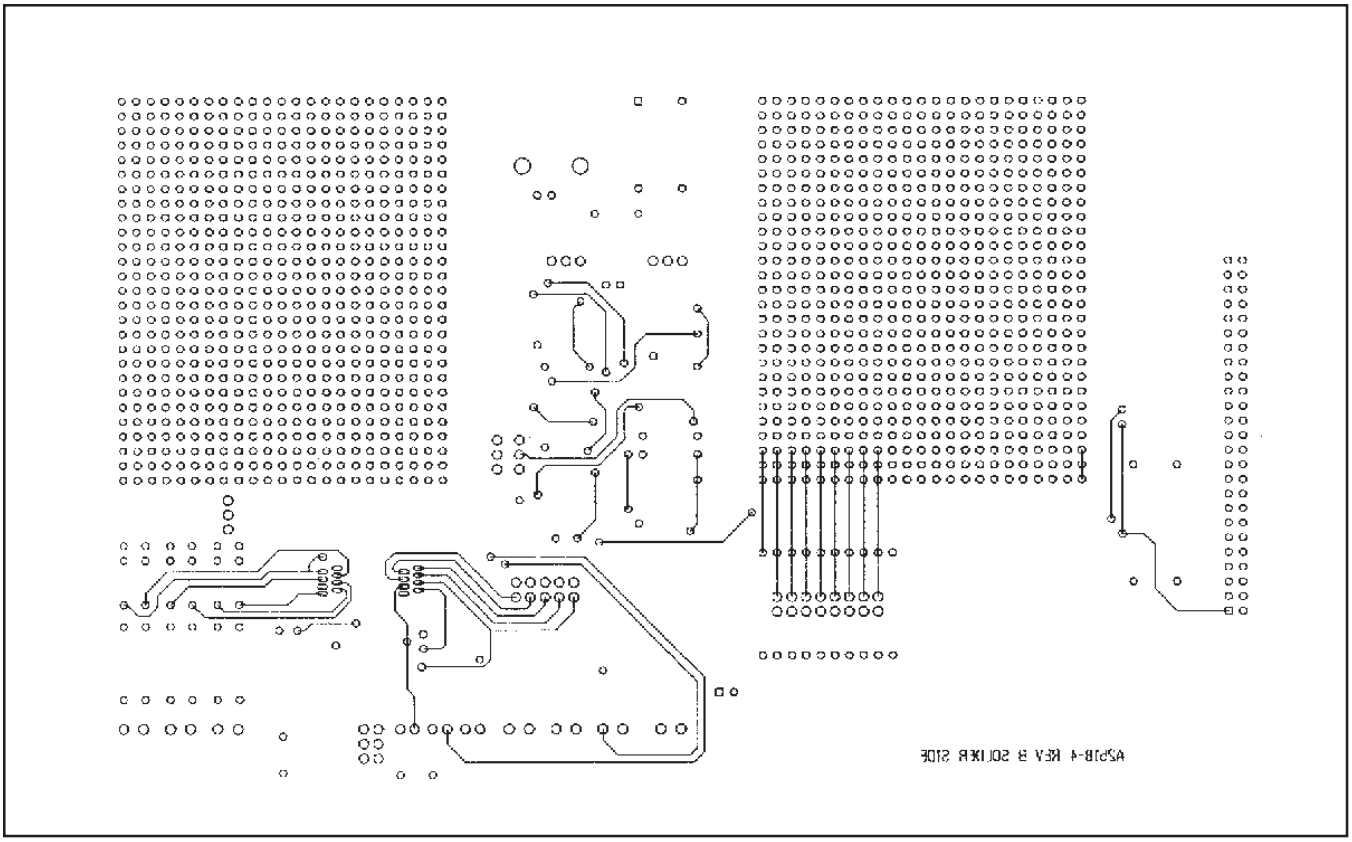


FIGURE 7. Solder Side of the DEM-ADS7843E/45E Demonstration Board.

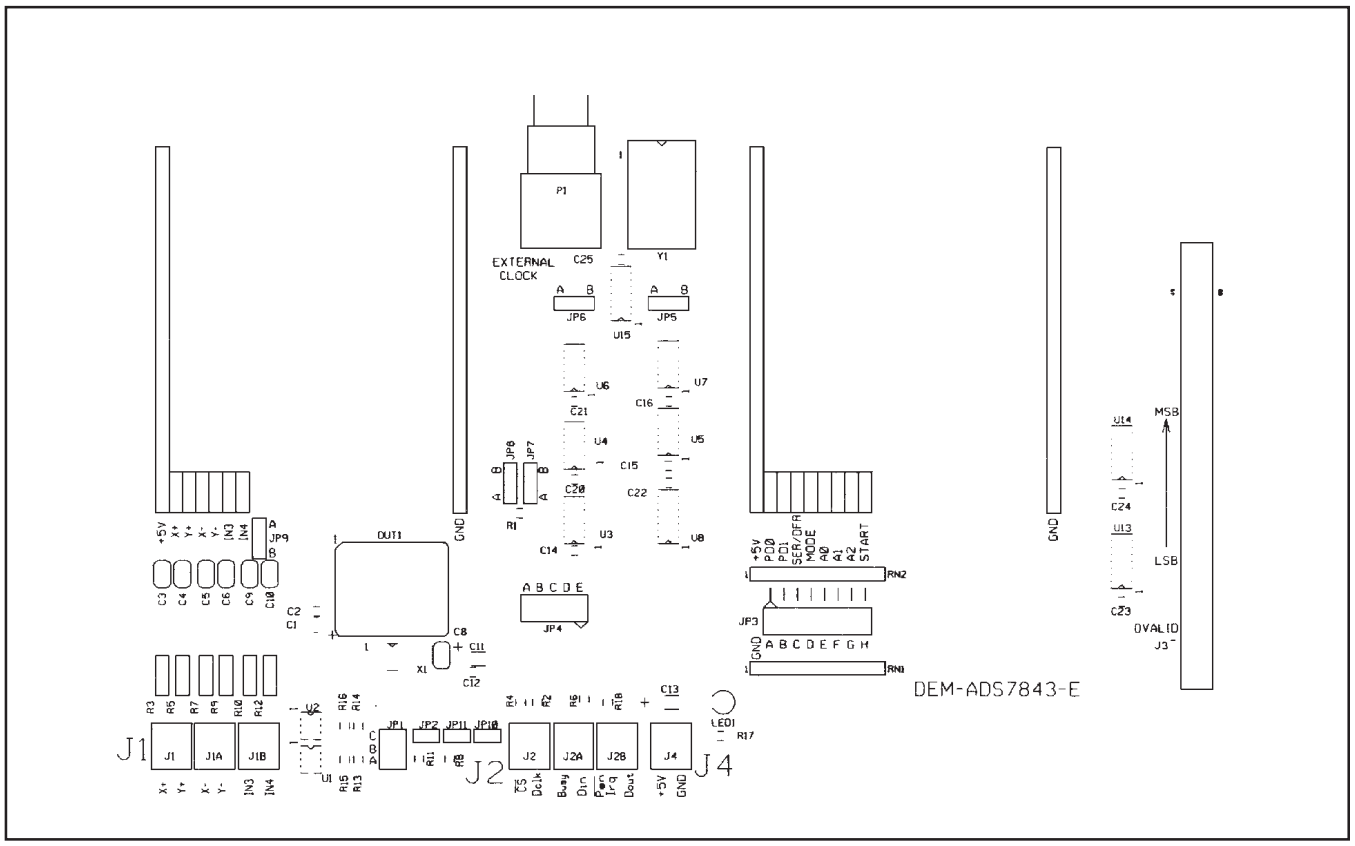


FIGURE 8. Component Side Silkscreen of the DEM-ADS7843E/45E Demonstration Board.

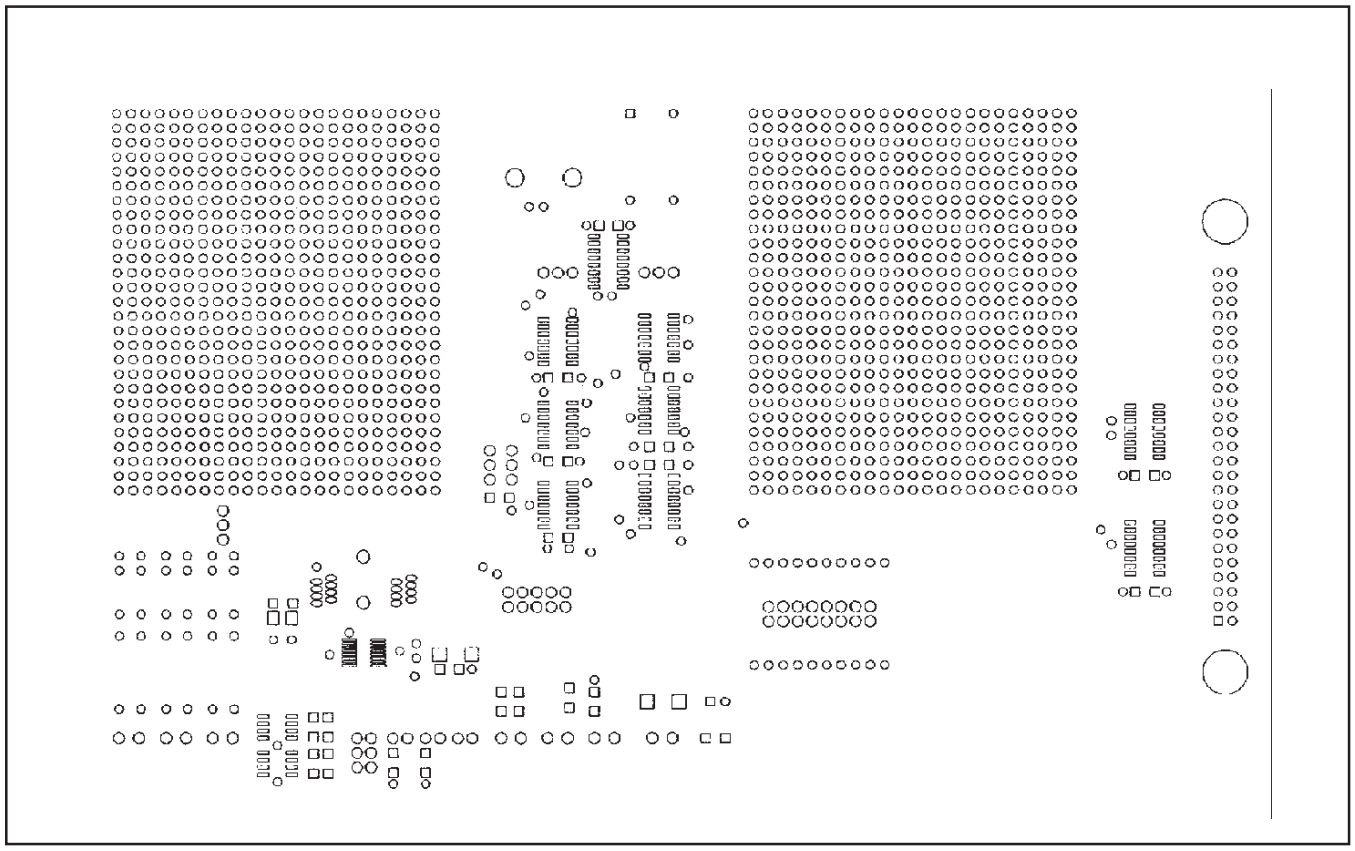


FIGURE 9. Component Side Soldermask of the DEM-ADS7843E/45E Demonstration Board.

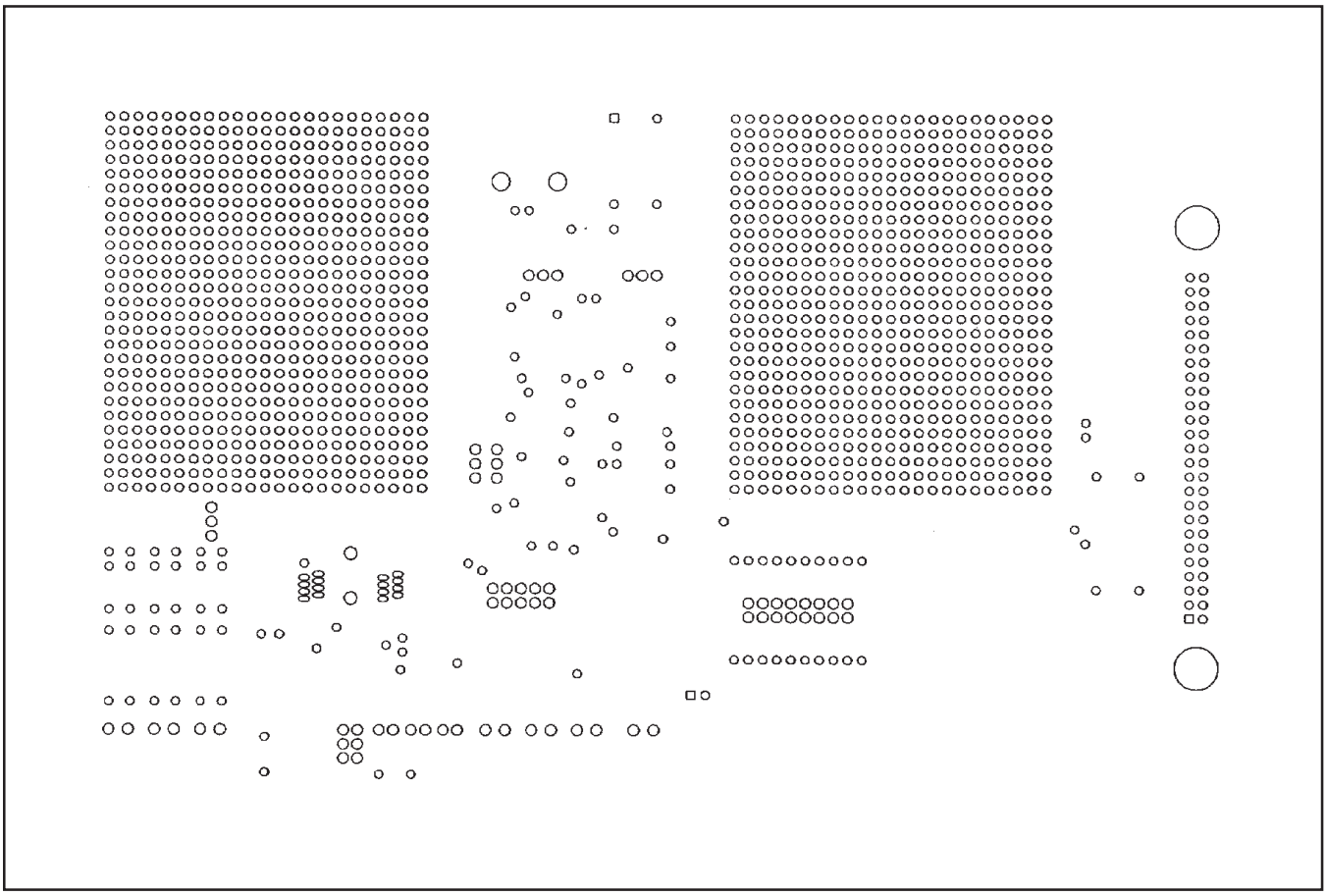


FIGURE 10. Bottom Side Soldermask of the DEM-ADS7843E/45E Demonstration Board.

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EVALUATING THE ADS7846 USING THE DEM-ADS7843E/45E EVALUATION FIXTURE

By Rick Downs

The ADS7846 is the next-generation version to the industry standard ADS7843 4-wire touch-screen controller. The ADS7846 is 100% pin-compatible with the existing ADS7843, and will drop into the same socket. This allows for easy upgrade of current applications to the new version.

Only software changes will be required to take advantage of the added features of direct battery measurement, temperature measurement, and touch-pressure measurement.

Since the ADS7846 has the same pin-out as the ADS7843, it can be evaluated using the DEM-ADS7843E/45E Evaluation Fixture, using the guidelines presented here.

INSTALLATION AND SET UP

The DEM-ADS7843E/45E is designed to allow evaluation using either the on-board clocking circuitry or in a stand-alone mode.

Stand-alone evaluation is done by removing all the jumper shunts of JP4, and using J1 and J2 for direct connections to the device-under-test (DUT).

Using the on-board clocking circuitry of the evaluation fixture, however, provides all the appropriate digital interface circuitry to drive the DUT Data Clock, Chip Select, and Serial Data In, which is coordinated with the BUSY and $\overline{\text{PENIRQ}}$ to provide serial and parallel output data.

The DEM-ADS7843E/45E has two positions on the evaluation board where the DUT may be installed. Position 1 is the socket, DUT1, on the board. The ADS7846 may be placed in this spring-loaded socket which allows the user to quickly swap in or out the device being evaluated. Alternatively, the DUT may be soldered onto the board in the X1 position.

The user must connect a +5V power supply to J4, and a 4-wire resistive touch screen to J1 and J1A. On the DEM-ADS7843E/45E, J1B is labeled as inputs IN3 and IN4; for use with the ADS7846, IN3 corresponds to the battery input (VBAT) and IN4 corresponds to the auxiliary input, IN.

REFERENCE VOLTAGE

The ADS7843 does not have an internal reference, therefore, the DEM-ADS7843E/45E provides three possible reference voltages on the board, which are jumper-selectable at JP1. Since the ADS7846 has an internal reference, no external reference is required. Therefore, to evaluate an ADS7846 in the DEM-ADS7843E/45E fixture, all the jumper shunts for JP1 should be removed, and the ADS7846 operated in differential mode.

EVALUATING THE ADS7846

With the hardware of the DEM-ADS7843E/45E set up as described previously, evaluation of the ADS7846 can begin.

In stand-alone mode, the user must supply the signals to the ADS7846 to access all its features. See the ADS7846 data sheet for help in developing software to drive the part.

Using the on-board clocking circuitry of the DEM-ADS7843E/45E, the user can test all the same features as the ADS7843, and can also access the extended feature set of the ADS7846. Using the jumper set, JP3, which allows the user to set the address bits in the control byte, the settings are then processed by a parallel-to-serial converter and transmitted to the DUT at the appropriate time under control of the on-board clocking circuitry.

TEMPERATURE MEASUREMENT

To read temperature data from the ADS7846, JP3 should be configured so that shunts on JP3A and JP3B are not installed (PD0 = PD1 = 1), JP3C is not installed (SER/$\overline{\text{DIF}}$ = 1), JP3D is installed (MODE = 0), JP3E, JP3F, and JP3G are installed (A0 = A1 = A2 = 0) and JP3H is not installed (S = 1). This configures the ADS7846 to read the on-board temperature sensing diode bias voltage at a bias current TEMP0. This voltage is typically 600mV at +25C, and has a temperature coefficient of –2.1mV/C. Thus, the temperature is given by:

$$°C = \frac{V_{TEMP0} - 600mV}{-2.1mV/°C} + 25°C$$

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This measurement of course is only as accurate as the initial 600mV reading; in actual use, the forward voltage of the diode would need to be measured at a known room temperature, and used as the initial offset in this calculation.

A second mode of temperature measurement is possible, which does not require an initial calibration. This method uses two temperature measurements to eliminate the need for absolute temperature calibration. This mode requires a second conversion of the diode voltage now at a bias current TEMP1.

The first measurement is made as described above for the single-measurement mode. The second measurement is then made by removing JP3E, JP3F, and JP3G, so that A0=A1=A2=1. The resulting voltage reading, V_{TEMP1}, is then used with the initial reading V_{TEMP0}, to calculate the temperature by:

$$\Delta V(mV) = V_{TEMP1} - V_{TEMP0}$$

$$°C = 2.68 \bullet \Delta V(mV) - 273°C$$

It is important to note that the difference in the voltage readings, ΔV, is expressed in millivolts.

BATTERY MEASUREMENT

The ADS7846 has the additional feature of being able to directly monitor a battery voltage, which can vary from 0.5V to 6V, even when the ADS7846 is powered from 2.7V, 3.3V, etc. The battery voltage, V_{BAT}, is internally divided down by 4 so that a 6.0V battery is represented as 1.5V to the ADC.

To perform a battery voltage measurement, JP3 should be configured so that shunts on JP3A and JP3B are not installed (PD0 = PD1 = 1). In addition JP3C is not installed (SER/$\overline{DIF}$ = 1), JP3D is installed (MODE = 0), JP3E and JP3G are installed (A0 = A2 = 0), but JP3F is not installed (A1 = 1) and JP3H is not installed (S = 1).

The resulting measurement is the battery voltage measured at IN3 on the DEM-ADS7843E/45E board, divided by four.

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